SEER® FOR HARDWARE

GALORATH

Inform decision making, evaluate design impacts, and assess risks. SEER® for Hardware (SEER-H™) is a comprehensive solution that can be used to build top-down parametric cost/schedule/effort estimates based on historical ranges or drawn from analogies or catalogs. Estimates may be built at a variety of levels to assess up-front project feasibility, optimize project costs and schedules, assess risk, and develop detailed project plans by providing a comprehensive preview of total cost of ownership for projects spanning:

- Mechanical, electrical, electronic, structural, and hydraulic hardware
- Components, subsystems, systems, and systems of systems
- Design, production, operations, maintenance (reliability), and disposal
- Development and production labor-hours and material costs, including prototypes
- Operations & Support costs and alternatives
- Estimated costs of competitive products

Key Features of SEER-H

Predictive Analytics built into SEER-H are models to compute labor hours, material costs and other costs based on hardware attributes such as weight, PCB count, heritage, quantities, learning curves and many other productivity factors.

Rate & Quantity models can be easily set up for rapid calculation of effort and cost when basic variables are known.

Extensive Reporting offering labor hours, labor cost, material cost, schedule, total, time phased to suit any output requirements. Custom reporting, data export, and PDF options are available.

SEER® FOR HARDWARE

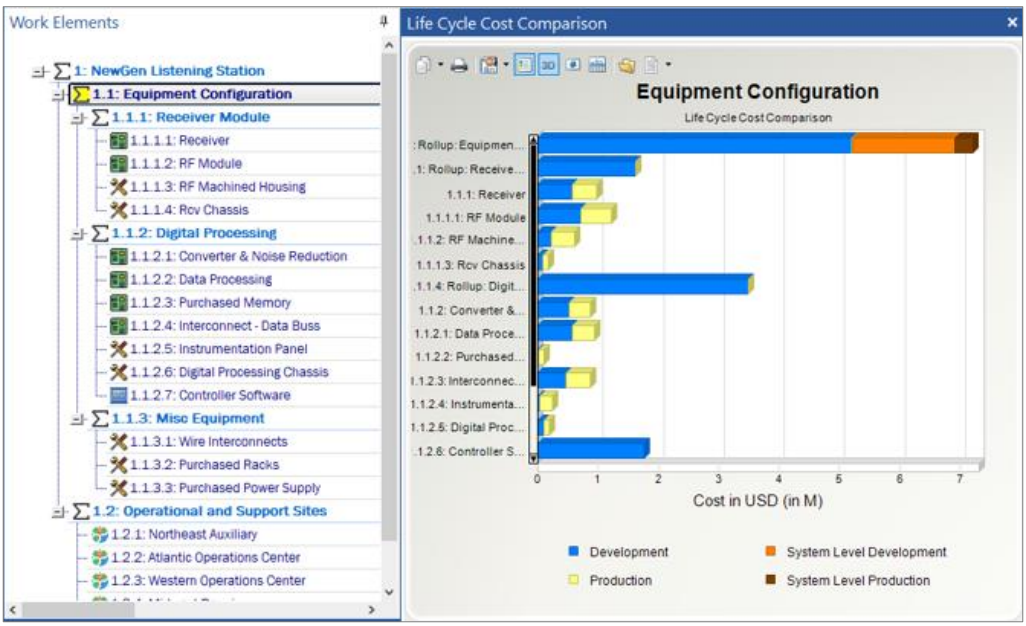
GALORATH

Electro-Optical Sensors option (SEER-EOS™) enables users to estimate the lifecycle costs of complex electro-optical sensors with much more accuracy and detail. EOS estimates are derived from user-selected technology options associated to the elements that comprise EO sensors (e.g., telescopes, focal plane arrays, and coolers), as well as specific values for key technical and performance parameters (e.g., telescope diameter and number of pixels).

Integrated Circuits option (SEER-IC™) simplifies the estimation of development and production costs for custom ICs, ASICs and FPGAs. SEER-IC enables accurate and reliable estimates specifying FPGA input variables such as Active I/O Pins per Chip, Clock Speed or Frequency, Active Logic Cells, New Design Percentage, Front and Back-end Complexity, and more. ASIC input variables include Process, Die Area, Feature Size (nanometers), Effective Gates per Die, Logic, Memory, and IP Logic Gates and Complexity, and more than 15 additional parameters.

Catalogs allow easy use and update of standard costs, task effort, labor rates and exchange rates.

Template Based Estimating through the Scenarios features to build consistent and complete estimates.



GALORATH.COM

info@galorath.com