SEER®
by GALORATH

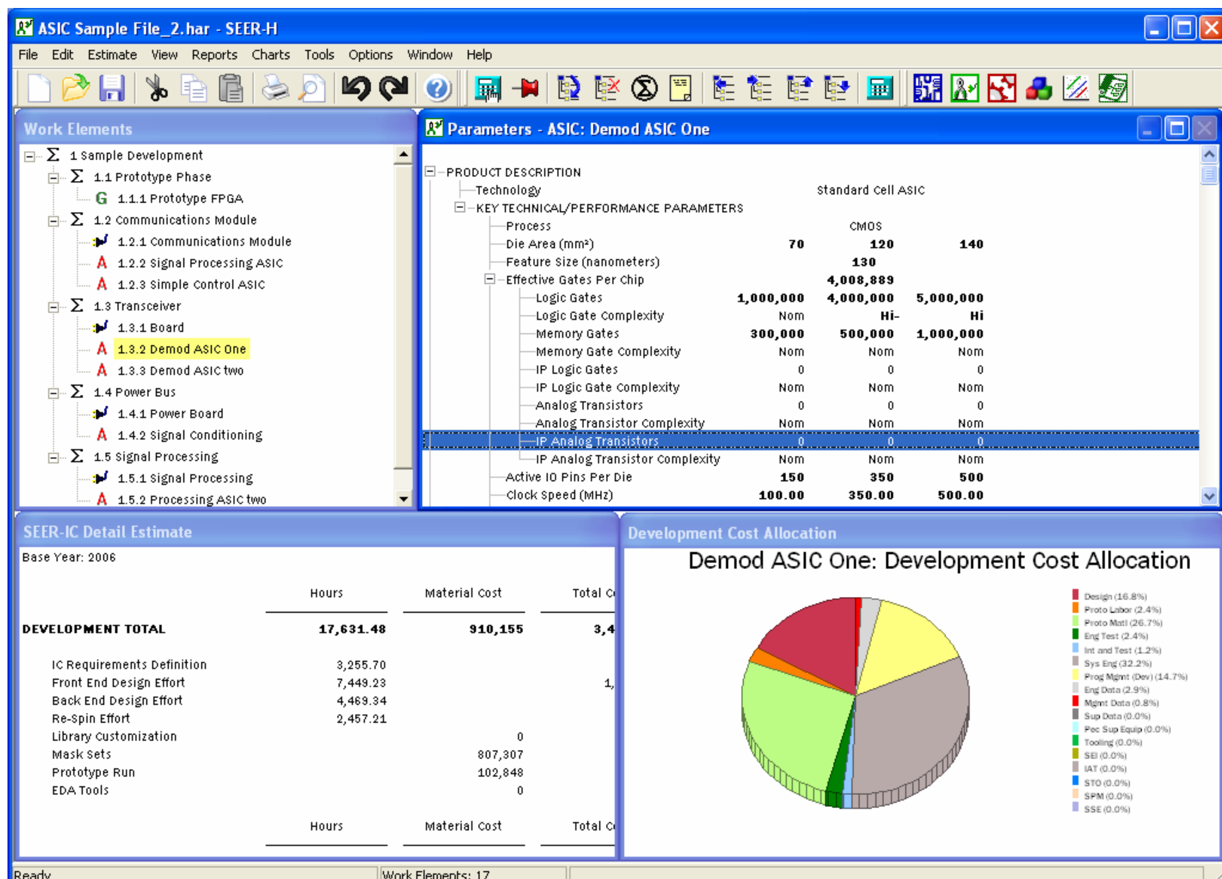
SEER-IC Plug-in for SEER-H

Dramatic increases in cost and complexity of custom components have made it imperative for Galorath to maintain a dedicated research program into the key cost drivers for this specialist area. Although SEER-H has the functionality to do approximations of IC costs at the PCB and Module level, the SEER-IC plug-in for SEER-H greatly enhances the users' ability to estimate these rapidly evolving technologies.

Many programs are dependent on the architectural approach applied to these key devices for their success. Recent post-mortem research studies conducted by Galorath demonstrate that accurate and reliable estimation of these technologies and their risks are vital to delivering programs on time and on budget whether in ground, airborne or space environments.

SEER-IC will simplify the estimation of development and production costs for custom ICs, ASICS and FPGAs.

Galorath are active in conducting many ASIC research/calibration studies and routinely presents findings to industry leaders. We have expended over two years of extensive research into current industry practices as well as utilizing many man months of consulting time from leading industry experts in integrated circuit technology and commercial practices.



Typical SEER-IC Parameters

FPGA input parameters	FPGA outputs
Active I/O Pins Per Chip Clock Speed or Frequency (MHz) Active Logic Cells New Design % Front End Complexity Back End Complexity Certification Level Developer Capability & Experience Development Tools & Practices Requirements Volatility Prototypes	Architectural Design Detail Design Simulation, Verification, and Implementation Floorplanning, Place, and Route (for advanced applications) Headcount Production total price
ASIC input parameters	**ASIC outputs**
Process Die Area Feature Size (nanometers) Effective Gates Per Die Logic Gates Logic Gate Complexity Memory Gates Memory Gate Complexity IP Logic Gates IP Logic Gate Complexity Analog Transistors Analog Transistor Complexity IP Analog Transistors IP Analog Transistor Complexity Active I/O Pins Per Die Clock Speed or Frequency (MHz) Wafer Diameter Package Type Radiation Level New Design % Complexity--Front End Design Complexity--Back End Design Certification Level Developer Capability & Experience Development Tools & Practices Requirements Volatility	IC Requirements Definition Front End Design Effort Back End Design Effort Re-Spin Effort Library Customization Mask Sets Prototype Run EDA Tools Unpackaged Die Package Assembly Final Test Qualification Test Minimum Buy Penalty Composite Yield Wafer Yield Qualification Yield Headcount Design Re-Spins Mask Steps Prototype Quantity

Galorath Incorporated
100 N. Sepulveda Blvd
Suite 1801
El Segundo
CA 90245

GALORATH

Galorath International Ltd
Peel House
Upper South View
Farnham, Surrey
United Kingdom
GU9 7JN